REMARKS

Claims 6-8 and 11-13 are pending in the application. Claims 1-5 have been canceled without prejudice. Claims 6, 11, and 13 have been amended by the present amendment. The amendments are supported by the specification as originally filed.

As an initial matter, the specification has been amended on page 7 to correct an inadvertent error in reference numeral 70". No new matter has been added.

Claim 13 was rejected under 35 USC 112, first paragraph, because the term "low resistance chip resistor" was not adequately described in the specification. Claim 13 has been amended to replace "low-resistance chip resistor" with "zero-resistance chip resistor." Use of a zero-resistance chip resistor in conjunction with the Applicant's invention is fully described in the specification (see, e.g., page 7, lines 15-18). Withdrawal of the rejection is respectfully requested.

Applicant's claimed invention is directed to a semiconductor package including an electrically-conductive bridge in the form of either a bonding wire (claim 6; see gold wire 90' in FIG. 6) or a chip resistor (claim 11; see chip resistor 90" in FIG. 7) for electrically connecting a corresponding via and bonding wire, which are not otherwise directly connectable due to the presence of an interposing electrically-conductive trace (e.g., trace 70A in FIGS. 6 and 7).

The electrically-conductive bridge recited in claims 6 and 11 spans in an overhead manner across the interposing electrically-conductive trace, leaving a gap between the electrically-conductive bridge and the interposing trace.

The above-described arrangements of an electrically-conductive bridge can be implemented in an easy and cost-effective manner by utilizing existing wire-bonding technology or surface-mounting technology (SMT), which allows via/bond finger bridging to be formed over a single-layer substrate, without having to use a multi-layer substrate.

Claims 6-8 and 11-13 were rejected under 35 USC 103(a) as being unpatentable over "Applicant's Prior Art Figures 3 and 4 (APAF)" in view of U.S. Patent 3,560,256 to Abrams. This rejection is respectfully traversed.

With reference to the Background section of the specification, prior art FIG. 3 shows an example in which bond finger 60B cannot be directly connected to via 80A using a continuous electrically-conductive trace (see page 3, lines 2-3); if such a direct connection were attempted, the interposing trace 70A would be impacted. Prior art FIG. 4 provides a solution to the problem of FIG. 3 by incorporating a multi-layer substrate; however, as discussed in the Applicant's specification, the use of a multi-layer substrate is undesirable due to its high cost and complexity (see page 3, lines 10-15).

Abrams fails to teach or suggest an electrically-conductive bridge with a gap formed between the bridge and an interposing trace.

With reference to FIG. 1 of Abrams, a circuit 20 includes a thick-film crossover conductor 26 connecting a pair of conductors 22a, 22b and being spaced from conductors 22c, 22d by a thick-film crossover dielectric 27 (see column 3, line 72 to column 4, line 2). The circuit 20 also includes a thin-film crossover resistor 28 connecting a pair of conductors 22e, 22f and being spaced from a conductor 22g by a thick-film crossover dielectric 29 (see column 4, lines 3-7). The crossover dielectrics 27, 29 are preferably glazes, and are made relatively thick so as to minimize capacitive coupling between crossing paths (see column 4, lines 64-70). The crossover dielectrics 27, 29 perform the function of minimizing capacitive coupling, which is of critical importance to the invention of Abrams.

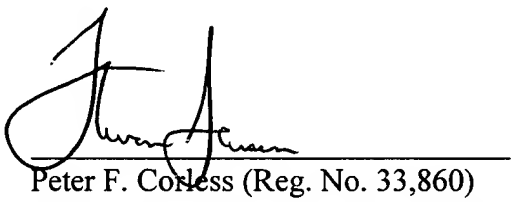
Abrams does not teach or suggest **a gap** formed between a bridge and interposing traces. In Abrams, the dielectric 27 is formed between the crossover conductor 26 and the interposing conductors 22c, 22d; similarly, the dielectric 29 is formed between the crossover resistor 28 and the interposing conductor 22g. Therefore, instead of forming a gap between the bridge and interposing traces, Abrams teaches that a dielectric must occupy this space.

Moreover, it would not be obvious to somehow provide "bridges" 26, 28 without their respective dielectrics 27, 29, as the dielectrics are critical to the purpose of "minimizing capacitive coupling between crossing paths" (column 4, lines 67-68), as taught in Abrams. Therefore, Abrams cannot be combined with "APAF" to produce the Applicant's claimed invention. Neither Abrams nor APAF, whether taken alone or in combination, teach or suggest an electrically-conductive bridge in the manner recited in claims 6 and 11.

The Applicant's claimed invention specifically recites that **a gap** is formed between the bonding wire and the interposing trace (claim 6), or between the chip resistor and the interposing trace (claim 11). As discussed above, the bonding wire and chip resistor can be fabricated using existing wire-bonding technology or surface-mounting technology (SMT). Therefore, the bridge can be fabricated in an easy and cost-effective manner, as compared to the prior art.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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Peter F. Corless (Reg. No. 33,860)
Steven M. Jensen (Reg. No. 42,693)
Dike Bronstein, Roberts & Cushman
Intellectual Property Practice Group
EDWARDS & ANGELL, LLP
P.O. Box 9169
Boston, MA 02209

Phone: (617) 439-4444

Customer No. 21874

APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph on page 7, lines 1-8 has been amended as follows:

The invention solves the foregoing problem of trace interposition by providing an electrically-conductive bridge 90 to span in an overhead manner across the interposing electrically-conductive trace 70A, and then electrically connecting one end of the electrically-conductive bridge 90 by means of a first trace 70' to the bond finger 60B and the other end of the same by means of a second trace 70" to the via 80A (note that if the first end of the electrically-conductive bridge 90 is directly bonded to the bond finger 60B, the first trace 70' can be eliminated; and if the second end of the electrically-conductive bridge 90 is directly bonded to the via 80A, the second trace [82] 70" can be eliminated).

IN THE CLAIMS

Claims 6, 11, and 13 have been amended as follows:

6. (Amended) A BGA (ball grid array) package, which comprises:

(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate, the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias, these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge as a bonding wire that spans in an overhead manner across the interposing electrically-conductive trace such that the bonding wire is free of interference with the interposing electrically-conductive trace and a gap is formed between the bonding wire and the interposing electrically-conductive trace, wherein the bonding wire has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

11. (Amended) A BGA (ball grid array) package, which comprises:

(a) a substrate having a front side and a back side;

(b) a semiconductor chip mounted on the front side of the substrate, the semiconductor chip having an array of bond pads;

(c) an array of solder balls implanted on the back side of the substrate;

(d) an array of bond fingers provided beside the semiconductor chip and which are electrically connected to the bond pads on the semiconductor chip;

(e) an array of electrically-conductive vias, each penetrating from the front side to the back side of the substrate and electrically connected to one of the solder balls;

(f) a plurality of continuous electrically-conductive traces for electrically connecting a first subgroup of the bond fingers to corresponding ones of the vias, these continuous electrically-conductive traces including at least one being interposed between a second subgroup of the bond fingers and their corresponding vias; and

(g) an electrically-conductive bridge as a chip resistor that spans in an overhead manner across the interposing electrically-conductive trace such that the chip resistor is free of interference with the interposing electrically-conductive trace and a gap is formed between the chip resistor and the interposing electrically-conductive trace, wherein the chip resistor has one end electrically connected to the corresponding via and the other end electrically connected to the corresponding bond finger.

13. (Amended) The BGA package of claim 11, wherein the chip resistor is a [low-resistance] zero-resistance chip resistor.

Claims 1-5 have been canceled without prejudice.